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Juler  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: : Tsiu Chiu Chan, et al.  
Serial No. : 09/160,824  
Filed : September 25, 1998  
For : STACKED MULTI-COMPONENT INTEGRATED  
CIRCUIT  
Group No. : 2826  
Examiner : T. Dickey

**BOX NON-FEE AMENDMENT**

Commissioner for Patents  
Washington, D. C. 20231

Sir:

**DECLARATION OF PRIOR INVENTION UNDER 37 C.F.R. § 1.131**

1. This declaration is to establish prior invention in this application filed in the United States (or a NAFTA or WTO country) at a date prior to August 20, 1998, which is the effective date of the reference (United States Patent No. 6,255,736) cited by the Examiner, and prior to March 2, 1998, which is the effective date of another reference of record in the application (United States Patent No. 6,150,724).

2. The persons making this Declaration are the inventors, Tsiu Chiu Chan, Arnaud Lepert and Lawrence Phillip Eng.

3. To establish the date of the invention of this application, the following attached documents are submitted herewith as evidence:

Invention disclosure form (7 pages).

4. The invention in this application was (1) reduced to practice at least as early as March 1, 1998, which is prior to the effective date of the cited reference; and/or (2) was conceived at least as early as March 1, 1998, which is prior to the effective date of the cited reference, coupled with due diligence from prior to the effective date of the cited reference to a subsequent reduction to practice or to the filing of the application. Upon information and belief, the invention in this application was reduced to practice before March 2, 1998 as evidenced in the attached documents. Also, upon information and belief, the effective date of the cited reference is August 20, 1998 and this application was filed on September 25, 1998, approximately thirty-six (36) days after the effective date of the cited reference, which evidences due diligence from prior to the effective date of the cited reference to the filing of this application. Further, upon information and belief, the effective date of the other reference is March 2, 1998 and this application was filed approximately six months after the effective date of the other reference, which evidences due diligence from prior to the effective date of the other reference to the filing of this application.

5. Upon information and belief, this Declaration is being submitted prior to final rejection.

6. As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURES:

Inventor: Tsiu Chiu Chan                      Date: \_\_\_\_\_

Inventor Residence: \_\_\_\_\_  
\_\_\_\_\_

Inventor Country of Citizenship: \_\_\_\_\_

Inventor Signature: \_\_\_\_\_

Inventor: Arnaud Lepert                      Date: \_\_\_\_\_

Inventor Residence: \_\_\_\_\_  
\_\_\_\_\_

Inventor Country of Citizenship: \_\_\_\_\_

Inventor Signature: \_\_\_\_\_

Inventor: Lawrence Phillip Eng      Date: \_\_\_\_\_

Inventor Residence: \_\_\_\_\_  
\_\_\_\_\_

Inventor Country of Citizenship: \_\_\_\_\_

Inventor Signature: \_\_\_\_\_

## INVENTION DISCLOSURE FORM

## COMPANY RESTRICTED WHEN COMPLETED

1. SITE Carrollton 2. GROUP ATO / OPL DIVISION Cont. J R D / DPL
4. PRODUCT CLASSIFICATION: Microprocessor: MMX (with multimedia); Signal Processor: SN  
Super Sampling; processing; Logic
5. DESCRIPTIVE TITLE OF THE INVENTION: Piggy Bank MEMORIES 3720 52012

## 6. INVENTORS:

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7. Date and location of first conception of invention: Jun 19, 1997 Carrollton, TX
8. Date of first written documentation or drawing of the invention Jun 19, 1997  
(Attach Copies)
9. Date and location where invention was first successfully reduced to practice \_\_\_\_\_

Describe how the invention was reduced to practice (model, on paper, etc.) and where model is located (if any): \_\_\_\_\_

From Page No. Piggy back memories (DRAM, FLASH, SRAM, etc)

1. Previously electronic systems (computers, cellular telephones, etc) were built with individual components that were assembled on a circuit board.

For example a computer requires -  $\mu$  processor

memory

I/O or bus interface

cache

Keyboard control circuits

Video circuits

Hard disk, hard drive, CD ROM circuits etc

Using the  $\mu$ processor for further illustration, it can be observed that the following evolution of combining more functions into the  $\mu$ p is occurring:

$\mu$  processor

$\mu$  processor + cache

$\mu$  processor + cache + I/O

$\mu$  processor + cache + DRAM

etc

Another example is the media 6X from Cyrix that incorporates the following into a single chip.

CPU to PLE

PLE to ISA

audio

memory control

graphics control

L2 cache

video memory

As the use of embedding a large memory core (like a DRAM) in a microprocessor or other large ASIC or sub system there will be a mixing of technologies to provide the end product.

a DRAM process plus an "ASIC" process (for  $\mu$ p)  
 FLASH process plus an "ASIC" process  
 SRAM process plus an ASIC process

From Page No. \_\_\_\_\_

this mixing of technologies will require a compromise for each of the components used

a DRAM process will be tuned specifically for DRAM;  
 requiring 2-4 poly layers and typically 1-3 metal layers  
 a SRAM process will be tuned specifically for SRAM;  
 requiring 2-4 poly layers and 2-3 metal layers  
 an ASIC process or one designed to support  $\mu$ processors will be  
 built specifically for logic and be composed of  
 1 poly & 4-5 metal layers

Depending upon the embedded application a process would have to  
 support for example (DRAM + microprocessor) etc

2-4 poly layer  
 + 4-5 metal layers

to satisfy requirement to build a DRAM memory cell &  
 the extensive interconnect required to route address lines  
 and data buses for 32, 64 or 128 bit  $\mu$ processors.

For illustration: ~~processor~~ to embed 16 meg in a 32 bit  
 microprocessor the device count would be as follows:

32 microprocessor	—	8 - 10 million transistors
16 meg DRAM x 32 bits	—	512 million transistors +
		512 million capacitors +
		— ? control logic
		more than 1034 million active devices

Obviously the economics to mix ~~processor~~ ~~with~~ DRAM & a microprocessor ~~might~~ would  
 be limited by the ~~capability of the process~~ ~~compromised~~ capability of  
 a "merged" process.

Instead of 16 meg x 32 bit & ~~32 bit~~ 32 bit  $\mu$ p in a monolithic device,  
 the technology would limit 512 k x 32 bit with a 32 bit  $\mu$ p.

To Page No \_\_\_\_\_

Witnessed &amp; Understood by me, \_\_\_\_\_

Date \_\_\_\_\_

Invented by \_\_\_\_\_

T. C. Chan - Arnold Dept  
 Leven Eng

Date 6/19/97



From Page No. \_\_\_\_\_

The limitation of this cost vs performance of merging functions like a microprocessor & DRAM or SRAM or embedding memories can be illustrated by the use of multichip carriers for the pentium or the circuit board for the pentium II.

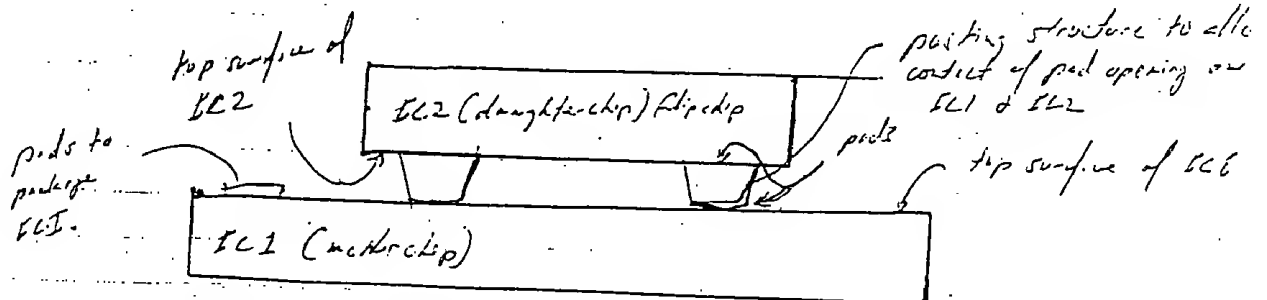
Package-multi - pentium CPU - single IC / heat issues  $\Rightarrow$  ceramic  
module - pentium pro - chip carrier with CPU & cache attached  
IC card - pentium II - CPU, multiple cache, control logic on PCB card  
epoxy  $\rightarrow$  bond flip into note board, heat.

While these solutions have provide cost effective methods to produce a higher level of integration, it reduces the performance that could otherwise be obtained in a monolithic solution (if it was available).

2. The invention disclosed here allows for optimization of cost & performance of individual components for to develop a electronic system or sub-system.

This in the case of combining a microprocessor with DRAM, the microprocessor can be manufactured in a process with a high level of interconnects (4-5 layers of metal) and the DRAM can be produced in process optimized for the DRAM memory cell & its least number of metal layers to ~~withstand~~ meet the product requirements (2-3 layers of metal).

First on IC it used a base to support another IC.  
Second, a second IC is piggy backed by flipping it so that its top layer of metal is exposed and available to make contact to the first.



Note: see Issue 957 EETimes - Microchip description

Witnessed & Understood by me,

Date

Invented by T. C. Chan

Recorded by \_\_\_\_\_

Recorded by \_\_\_\_\_

To Pa

Date 6/19/97

100

From Page No. \_\_\_\_\_

This invention allows the following

1. To combine 2 or more IC's into <sup>one</sup> compact structure ~~which~~ <sup>over</sup> integration ~~and~~ chip carriers (pick-up solutions) or PC boards.
2. allows individual component to be manufactured ~~with~~ <sup>using</sup> the process and technology to optimize the speed, performance, cost, of that component, i.e. DRAM process or µp or ASIC process or flash vs SRAM ...
3. allows "higher integration" of components that otherwise might be limited for an embedded application, ~~where~~ <sup>where</sup> the process is expanded to support requirements of individual components or if there was process incompatibility

byte width - 16

32

64

128 etc

DRAM process (4p/2mil) + µp or ASIC process (1p/4.5mil)

4p/4.5mil common ~~or~~ merged process

4. Improves performance of the function by elimination packaging or wiring delays with IC to IC direct contact. High speed transmission in the 500 mbz to 71 gig can be supported and achieved with this concept.

Witnessed &amp; Understood by me, \_\_\_\_\_

Date \_\_\_\_\_

Invented by T. C. Chien <sup>Hand Signed</sup>

Loren Fan

Date 6/19/97

To Page No. \_\_\_\_\_



## What's Hot

### THE BIG DAC ATTACK

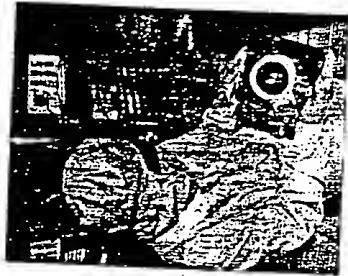
The 34th Design Automation Conference opens today in Anaheim with notable interactive design activity already afoot. An ambitious Web site called Electronics Design & Technology Network will be introduced at the show. The "one-stop shop" for engineers, created by a new joint venture between Aspect Development and CMP Media Inc., can be found at [www.edtn.com](http://www.edtn.com). Page 16. Formalization of the Digital Design Alliance will demonstrate a Web-based tool at the show that lets design engineers combine the company's formalization methodologies over the Web. It's at *EE Times* online's "EDA Advantage" column at [techweb.cmp.com/eda/advantage/advantage.html](http://techweb.cmp.com/eda/advantage/advantage.html). Page 8. *EE Times* also continues its coverage of the show with a report on next-generation design languages. Page 57.

### ADDED FOCUS FOR STN LCDs

Sharp Corp. has revitalized its twisted-nematic (STN) LCDs for multimedia display by developing a driving method called High Contrast Ad-



### X-ray lithography approach anticipates optical advances



An IBM operator loads a 1-GbH DRAM test mask into IBM's e-beam lithography system. The company's ultimate goal is to bring the entire process down to 0.1 micron and below, using a single lithographic process. To accomplish that, IBM researchers have tapped a variety of specialized techniques to push down the channel length of CMOS-based devices. See story, page 35.

## ATM comes under attack in the WAN

**By Loring Wibel**  
NEW ORLEANS — The advocates of new means — The advocates of networking gear based on the increasingly pervasive Internet Protocol are taking their fight into the last perceived bastion of asynchronous-transfer-mode signaling technology: the wide-area public network. While ATM is by no means dead, the Internet Protocol (IP) is extending its reach further than previously thought, and a broad class of network-equipment designers may have to support both approaches. The central-office DSL access multiplexer (DSLAM) was supposed to have been the point at which IP traffic would be routed, but now it's being challenged by ATM.

### ANALYSIS

Licenses for the Ipsilon Flow Management Protocol (IFMP) and Generic Switch Management Protocol (GSMP) will let DSLAM managers control and prioritize network equipment. See story, page 16.

Mentor, Synopsys, Cadence roll ambitious systems-on-silicon strategies

## EDA mounts response to SOS call

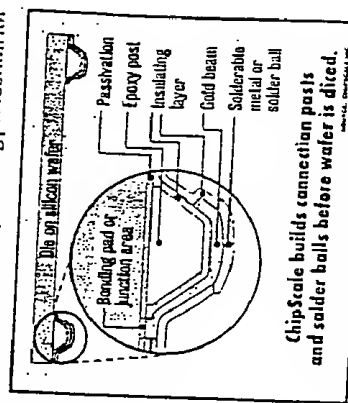
## Two firms put contacts on wafer-bound dice

## Chip-scale steps up as wafers grow legs

By Terry Costlow

SAN JOSE, CALIF. — Chip-scale packaging may take off sooner than expected with the emergence of techniques for putting contacts on a chip while it is still in wafer form. The wafer-level work, being performed at two companies, will help vendors take chip-scale packaging beyond low-lead-count devices to more-complex components, in which the space-saving benefits of chip-scale become even more pronounced.

ChipScale Inc., for one, is finalizing technology that will permit the production of ICs, power MOSFETs and integrated passives in chip-scale packages. "One advantage is that with wafer-level processing of our post and beam technology, we can create different size contacts for power, ground and data," said Jim Young, marketing vice president at ChipScale. "We can also do full wafer-level testing without



the die without adding the bulk of conventional packages. Until now, however, the company has only made headway by signing licenses and helping forge standards for low-lead-count devices with fewer than 28 contacts. Other chip-scale firms are also

► CONTINUED ON PAGE 160

Comdex buzz: HPD-matched

Pl's n  
a Cq  
of W  
"Feb  
A q  
Raid  
bbs

Contacts are attached while ICs are still on the fab line

# Chip-scale packages move to wafer-level assembly

► CONTINUED FROM PAGE 1

turning to wafer-level assembly. Tessera Inc. (San Jose, Calif.), which has licensed its chip-scale packaging to Intel, Texas Instruments, Hitachi and other companies, is also gearing up to put contacts on the chip while it's still in wafer form.

"What happens now is that you can have a wafer fab facility that ships packaged wafers, which saves the fab guys about 20 days in processing," said John Smith, chief executive officer at Tessera. "This also gets rid of a very expensive tester."

If wafer-level production indeed catches on, it may provide several significant benefits to semiconductor manufacturers. "Today, for example, many spend a fair amount of time and money sending die to IC packaging houses to the Far East, sources said.

"Wafer-level assembly makes it really convenient to do packaging, which could be a major benefit for semiconductor manufacturers," said Jan Vardaman, president of TeclSearch Inter-

national (Austin, Texas). "Potentially, they could bring assembly closer to the semiconductor fabs. It will be fairly easy for chip makers to do their own packaging."

None of the licensees of either ChipScale or Tessera is yet producing parts that use the wafer-fabrication processing, however, but both expect to see initial shipments this year. This rampup will come as chip-scale packaging moves forward swiftly, even though usage in the United States is still only in prototype stages.

"We haven't run our numbers yet, but it looks like shipments will be in the tens of millions this year," said Vardaman. That "is quite an increase over last year, when they were just a few shipments, mostly in Japan," he said. "The big holdup this year will be to get production volume up. Demand is definitely there, especially for flash memory in chip-scale packages."

Most observers and suppliers agree that the main reason system designers turn to chip scale is to

pack more into small products such as cell phones, notebooks and video cameras. However, one contract manufacturer who has done a number of prototype boards has found a surprising side benefit beyond size.

"We can place them on boards faster than plastic BCAs or TSOPs because they are small

**But higher lead counts—and their benefits—remain over the horizon.**

enough to put in a clip shooter," said Julian Partridge, senior R&D engineer at XelTel Corp. (Austin). "This is a self-centering package, so the chip shooter can place them precisely enough even at fairly fine pitches."

Though ChipScale and Tessera are talking about high lead-count ICs, both firms are currently working more with middle-densi-

ty packages. Most of the chips that will use this new packaging technique will have fewer than 200 leads. However, they are being used in a wide variety of ICs.

"We are starting to ship all types of chips—mixed-signal, ASICs and DSPs—with pin counts of 60 to just shy of 200 leads," said Kurt Wachter, packaging strategy manager at Texas Instruments' Semiconductor Group (Dallas). "This attack what is currently going into thin quad flat packs. I feel it will displace TQFPs when it gets cheaper. And I think it can be cheaper when volumes get there. This is a different beast than the plastic BCAs that go into PCs and workstations, which have much higher lead counts."

One reason that clip-seal packages are seeing use mainly in fairly low lead-count applications is that the contacts are fairly close together. That means that routing signal lines to a high number of contacts will be difficult unless a board's line widths are quite fine.

"Clip-scale's real benefit will

be in high lead-count packages, but it's only being implemented in low pin counts because people don't know that the line widths they need for higher lead counts are available," said Marshall Andrews, chief executive officer of ITRI (Austin), an R&D center in the circuit board industry.

"In one year, we've gone from three companies who could make buried vias or 'build-up' boards to 20 who have the capability now."

However, these microvia or build-up board technologies are more expensive than conventional laminate board-plating techniques. That's one of the criticisms some people have leveled against wafer-level contact placement: If leads are produced at that level, it's more difficult to fan them out to a roomier pitch.

"A big problem with chip-scale is that the die size is the size of the package, which means a customer has to deal with pitches of half a millimeter or below," Wachter said. "That means that they have to use more expensive printed-circuit boards."

# Net-protocol backers invade ATM's home turf

► CONTINUED FROM PAGE 1

IP traffic to serve most service mixes, said Larry Blair, vice president of marketing at Jpsilon.

sense that we are very much aware of what they're doing."

DSLAM could be seen as the last stand in wide-area public network. For the full ATM storyline

ATM proponents remain adamant about the inability of a packet service to provide guaranteed bandwidth in a given time slot. "No one will know how this

become even more critical in the DSLAM as carriers' designs shift from DSLAMs to what Cooper calls the DSLAS, or digital-subscriber loop access switch. He

based on ATM protocols. FlowPoint has developed routers that route IP traffic over ADSL lines, and it has workstation systems with ATM communication and conversion